


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Bhattacharya et al.

Serial No.: 09/896,071

Filed: June 29, 2001

For:  PROCESS FOR AUTOMATED GENERATION OF DESIGN-SPECIFIC COMPLEX FUNCTIONAL BLOCKS TO IMPROVE QUALITY OF SYNTHESIZED DIGITAL INTEGRATED CIRCUITS IN CMOS

Notice of Allowance Date: 10/31/2005

Examiner: Thuan V. DO

Group Art Unit: 2825

Confirmation No.: 9529

Customer No.: 27,623

Attorney Docket: 162.7106USU

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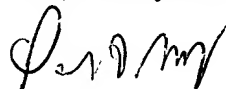
CORRECTION OF INFORMALITIES

Dear Sir:

In response to the informalities enclosed with the Notice of Allowability dated October 31, 2005, enclosed herewith are the formal drawings (7 sheets) for Figures 1 thru 7c for the above-identified patent application.

Please charge any additional fees or credit any such fees, if necessary to Deposit Account No. **01-0467** in the name of Ohlandt, Greeley, Ruggiero & Perle. A duplicate copy of this sheet is attached.

Respectfully submitted,



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Date: November 29, 2005

CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: MAIL STOP ISSUE FEE, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, ON November 29, 2005.

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